A proposed low-cost radiation dosimetry system using commercially available dynamic random-access memory (DRAM) modules

Stefan Nikolaj, January 19th 2023

Summary

This article will discuss my idea of using dynamic random-access memory to measure radiation, some background information and history, as well as a proposed algorithm and test setup. Unfortunately, I could not finish it, as I do not have a source of alpha particles to test it with.

Introduction

All computers use random-access memory (RAM) for temporary storage of data. There are two main types of RAM – dynamic RAM (DRAM) and static RAM (SRAM) which differ in their physical construction and memory density. Dynamic RAM is built out of repeating floating gate metal-oxide semiconductor field-effect transistors (MOSFETs) – a three-terminal device which acts as a simple electronic switch. When a charge is present at the gate terminal of the MOSFET, it presents a low-resistance current path, while the lack of a charge presents a very high resistance. The gate acts as a capacitor and can "hold" electrons indefinitely in theory, and for a few milliseconds-seconds in real life, depending on the size of the gate. DRAM is essentially an array of such transistors, with the charge at the gate used to hold the data. In terms of DRAM structures, the gate is referred to as the "well" of electrons. When the well is filled, the cell holds a value of "0", and when empty, the cell holds a value of "1".

The effects of radiation on DRAM structures has been widely studied since 1974 [1, 2], when Intel discovered that its 2107 DRAM integrated circuit (IC) often had random "bit-flips" – changes in the value of one bit (one transistor) during operation. It was later discovered that these events, called "soft errors," were specifically due to impurities in the materials used to encapsulate the DRAM ICs, which contained trace amounts of alpha-particle-emitting uranium and thorium isotopes [1]. Alpha particles are simply the results of radioactive decay which releases a helium nucleus made up of two protons and two neutrons. These positively charged particles have a very high speed (of 0.05c), travel in straight lines, and are difficult to physically stop [1]. A collision with a DRAM cell would result in electron-hole pairs being created, which would fill a well with electrons where there were none before and cause a change from a "1" to a "0". Further research shows that for later models, a change in both directions could be observed at approximately an equal rate, indicating that the internal physical organization of the structures in the IC was changed, however the basic mode of operation of DRAM has remained unchanged [3]. At the time of the Intel study, the largest DRAM available was 64KB, while each gate required between 300 000 and 3 000 000 electrons to hold data [1]. By 1996, this number had shrunk to 40 000 electrons [4], and DRAM structure sizes are continually shrinking. Simultaneously, due to the increase, DRAM capacity has drastically increased. Today, DRAM ICs with sizes up to 128Gb are available for purchase – while they have approximately retained the same size as the original 64KB DRAMs in the original breakthrough paper. Due to this, modern DRAM ICs are much more susceptible to alpha-particle-induced soft errors – so much so, that they use multiple algorithms to counter soft errors, such as error-correcting code (ECC) [2]. However, it is important to note that the adoption of ECC has mostly been relegated to high-reliability spaces such as servers and mainframes, while personal computers are still vulnerable to alpha-particle-induced bit flips.

Interactions between alpha particles and RAM

In real life, most of these alpha-particle-induced soft errors result from cosmic rays, which split apart in multiple particles when they enter and interact with earth's atmosphere – creating alpha particles among other types of particles such as pions and muons [5]. The effects of these cosmic rays increase strongly with altitude, and this has been a known issue for high-altitude systems which depend on computers, such as planes [2, 5]. Apart from alpha particles, DRAM cells are also vulnerable to low energy neutron interactions with boron-10. This isotope which exists in relatively high (19.9%) abundance is reacts with neutrons by splitting apart and releasing a lithium-7 atom and an alpha particle [5]. Boron is present in semiconductor devices as a p-type dopant in silicon. As a result of the aforementioned property, boron-10 has been used for radiation measurement.

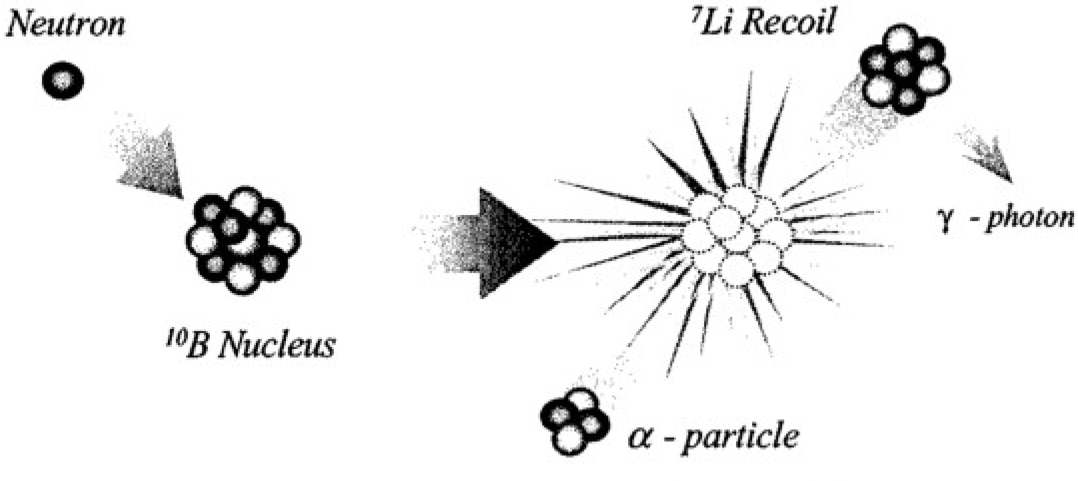

Figure 1: Boron-10 interaction with neutron [5]

The soft errors caused by these interactions are usually non-destructive and known as a single-event upset (SEU) – as are the aforementioned bit flips. These changes disappear whenever the data stored in the cell is overwritten with new data and do not permanently affect the device [5]. However, other events can be much more destructive. Imagine, for example, a CMOS push-pull gate where only one MOSFET is biased. An alpha particle could interact with the gate of the other MOSFET, turning it on and creating a short circuit between the power rails and ground. If the DRAM is not immediately powered off or if the error is not detected by power management circuitry, this could overheat and permanently damage the IC.

Viability of DRAM banks as radiation detectors

However, what if this property of alpha particle sensitivity was used to detect radioactive events? Starting in the early 1980s, designs for low-cost particle detectors using DRAM were proposed, and some were successfully implemented [3]. At the time, DRAM sizes were still relatively small to what they are today, while prices were quite high [6]. Prices since then have fallen and capacity has increased, meaning that large-capacity DRAM (or even SRAM, which is out of the scope of this article) banks for detecting radiation are currently viable with some prototypes already in existence [5, 6].

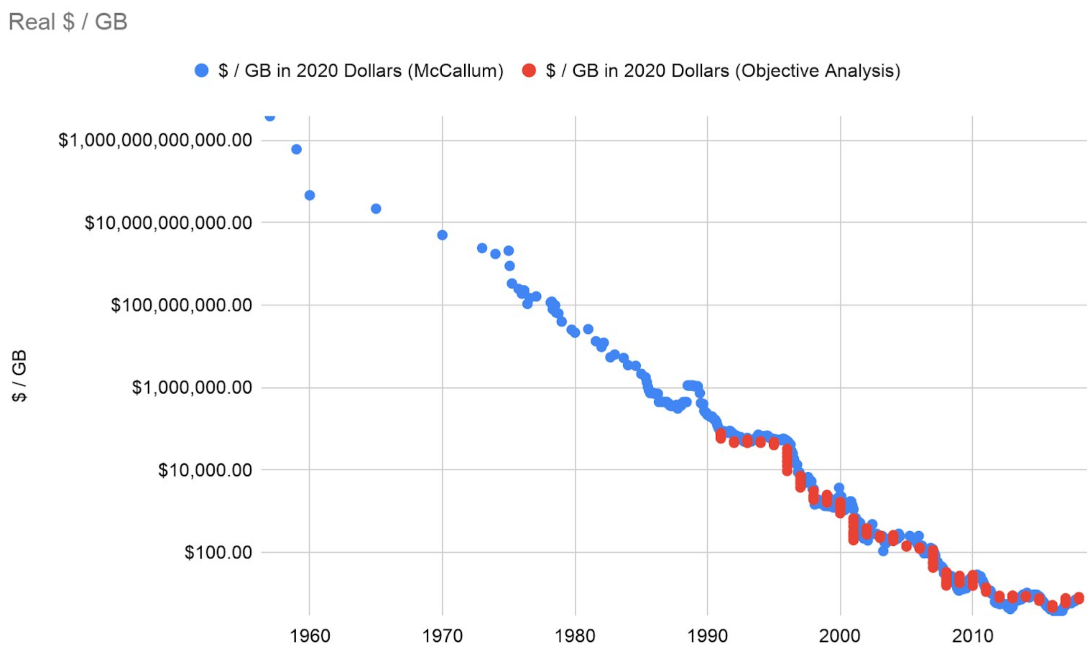

Figure 2: Historical trends of DRAM prices

Types of contemporary radiation measurement

There exist many types of radiation dosimeters in use today [7]. Most of these dosimeters are electronic dosimeters which either use thermoluminescence effects or MOSFETs. The MOSFET type uses the same alpha particle effect present in DRAM, however in the case of the MOSFET detector, the alpha particle interactions create electron-hole pairs in the gate which changes the threshold voltage of the MOSFET. With appropriate sensing circuitry and MOSFET choice, this can result in a linear and accurate radiation detector [8]. However, the types of MOSFETs often used for this purpose are ones whose characteristics are subject to change, and many common types – such as power MOSFETs – have a complicated internal structure which does not allow measurement of these effects [8]. Furthermore, datasheets scarcely mention the data points necessary to choose an appropriate MOSFET for the task, meaning that these can be difficult to source in an environment of scarcity, and as modern MOSFETs gain more features and grow in complexity, they may only become harder to design from scratch.

The advantage of DRAM

Theoretically, DRAM should retain the same advantages as MOSFET-based dosimeters. Linearity would be achieved through the fact that alpha particle impacts from the same source will approximately impact the same number of DRAM cells per particle [1]. An even bigger advantage would be provided by the wide availability of DRAM, which is present in all personal computing devices in large quantities, and most laptops and desktop computers have it in removable, standardized packages (DIMM/SODIMM). Furthermore, neutron-alpha particle converters such as boron-10 could be used to amplify a neutron source, as has been proposed [3].

Testing algorithm

DRAM, unlike SRAM, is somewhat complicated to work with in a circuit [3]. Due to the leakage present in all capacitors, DRAM cells must be constantly refreshed to keep their memory. For the purposes of maximising detection of SEUs, the refresh rate was chosen to be the maximum refresh rate specified for the DRAM cell in question. Furthermore, DRAM cells often use multiplexed address and data buses, which complicates the necessary circuitry. As a result, the proposed system has two algorithms – one to handle the physical needs of the DRAM circuit itself, and another to detect errors. Because of the possibility of bit flips occurring in both directions, the algorithm was designed to accommodate both “0” to “1” and “1” to “0” bit flips in an alternate fashion. Since DRAM requires only microseconds to detect an event, the rate at which the algorithm can choose either all “1”s or all “0”s can be in the range of seconds.

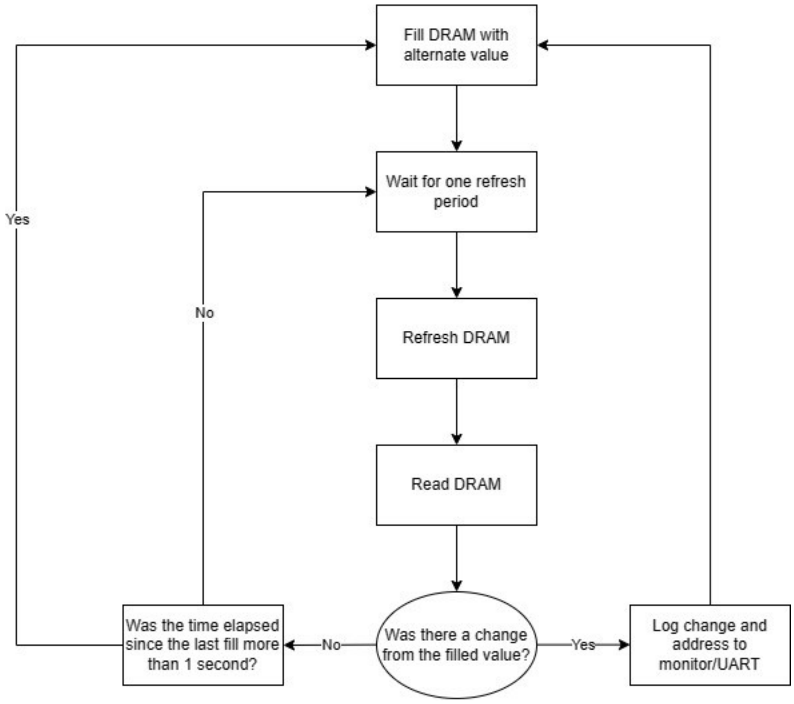

Figure 3: Algorithm for error testing

For the physical hardware, a system using an FPGA is proposed, with the method used to refresh the DRAM being a full read cycle with hidden refresh every 16ms as per the datasheet of the model of DRAM used[9, 10], which was one that was immediately available – a SIMM stick of 1MB DRAM containing two GM71C4400BJ60 DRAM ICs manufactured in 1996. The write algorithms were identical to the read algorithms apart from the assertion of the #WE pin instead of #OE.

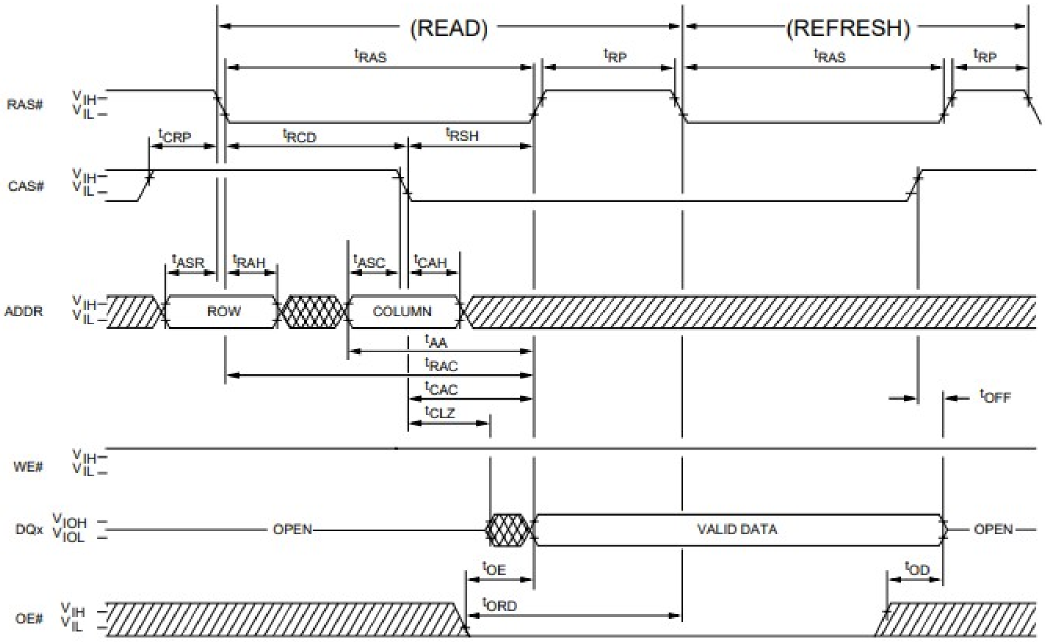

Figure 4: Read cycle illustrated

This is all very cool, except that I can neither afford a physical FPGA nor a radiation source. Also, I’m not very good with VHDL, since I can’t afford an actual FPGA. Hopefully I can get into a good college and be overjoyed by a generic 100$ Terasic DE-10 Nano I have to pay 80000$ per year to get to use. C’est la vie.

Resources:

[1.] T. C. May and M. H. Woods, “A new physical mechanism for soft errors in Dynamic Memories,” *16th International Reliability Physics Symposium*, 1978.

[2.] R. J. Peterson, “Radiation-induced errors in memory chips,” *Brazilian Journal of Physics*, vol. 33, no. 2, 2003.

[3.] P. J. Winters, “The radiation soft dynamic RAM as a particle detector,” *IEEE Transactions on Nuclear Science*, vol. 30, no. 1, pp. 540–542, 1983.

[4.] A. S. Huang, “Bunnie's RAM FAQ,” *Bunnie's DRAM FAQ*, 28-Jun-1996. [Online]. Available: http://web.mit.edu/rec/www/dramfaq/DRAMFAQ.html. [Accessed: 19-Jan-2023].

[5.] K. Jiang, “Design of SRAM based dosimetry used for neutron and proton detection,” M.S. thesis, University of Waterloo, Ontario, Canada, 2020. Available: https://uwspace.uwaterloo.ca/bitstream/handle/10012/15791/Jiang_Kai.pdf.

[6.] A. Bergal, “Trends in DRAM price per gigabyte,” *AI Impacts*, 15-Sep-2020. [Online]. Available: https://aiimpacts.org/trends-in-dram-price-per-gigabyte/. [Accessed: 19-Jan-2023].

[7.] “8 categories of radiation dosimeters for dose and exposure monitoring and worker safety,” *8 Categories of Radiation Dosimeters for Dose and Exposure Monitoring and Worker Safety - Radiation Emergency Medical Management*, 19-Jan-2023. [Online]. Available: https://remm.hhs.gov/radiation-dosimeters-dose-monitoring-worker-safety.htm. [Accessed: 19-Jan-2023].

[8.] O. F. Siebel, J. G. Pereira, M. C. Schneider and C. Galup-Montoro, "A MOSFET dosimeter built on an off-the-shelf component for in vivo radiotherapy applications," 2014 IEEE 5th Latin American Symposium on Circuits and Systems, Santiago, Chile, 2014, pp. 1-4, doi: 10.1109/LASCAS.2014.6820261.

[9.] Micron Technology, “Various methods of DRAM refresh,” Feb-1999. [Online]. Available: https://downloads.reactivemicro.com/Electronics/DRAM/DRAM%20Refresh.pdf. [Accessed: 19-Jan-2023].

[10.] LG Semiconductor, “GM71C(S)4400C/CL datasheet,” *Alldatasheet*. [Online]. Available: https://pdf1.alldatasheet.com/datasheet-pdf/view/122768/LG/GM71C4400CLR-70.html. [Accessed: 20-Jan-2023].